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Docket Number (Optional)
260/085

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Technology Center 2100

In re Application of: Bulent Dervisoglu, et al.

Application No. 09/765,958

Filed: 01/18/01

For: HIERARCHICAL TEST CIRCUIT STRUCTURE FOR CHIPS WITH MULTIPLE CIRCUIT BLOCKS

The owner*, Cadence Design Systems, Inc. of 100% percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application, which would extend beyond the expiration date of the full statutory term defined in 35 U.S.C. 154 and 173, as presently shortened by any terminal disclaimer, of prior Patent No. 6,631,504. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

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2. ☒ The undersigned is an attorney of record.

Janet D. Chance April 6, 2004

Signature

Date

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